UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,781	07/24/2003	Jerry L. White	SC12522ZP	1178

23125 7590 10/31/2006

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
LIEW, ALEX KOK SOON	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,781	WHITE ET AL.	
	Examiner	Art Unit	
	Alex Liew	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,16-21 and 24-30* is/are rejected.

7)☒ Claim(s) *14,15,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 14, 15, 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regards to claim 14, the examiner's search shows there is no applicable prior art and suggestions disclosing *repeating* the sectioning of the prepared device sample to facilitate viewing another cross-section face of the device under inspection, and performing dark field analysis on the another cross section face of the prepared device sample with the use of dark field illumination in combination with claim 1.

With regards to claim 22, see the rationale for claim 14.

With regards to claim 15, the examiner's search shows there is no applicable prior art and suggestions disclosing prior to preparing and sectioning the device sample, performing an initial assessment of the device under inspection with the use of acoustic scanning to determine *a location for cross sectioning* the device sample, the location corresponding to a potential failure area or point of delaminating in the device sample in combination with claim 1.

With regards to claim 23, see the rationale for claim 15.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4 – 8, 10 – 13, 16, 17, 19, 20, 21 and 24 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over DePetrillo (US pat no 6,342,400) in view of Nishimura (US pat no 5,761,337).

With regards to claim 1, DePetrillo discloses a method for performing failure analysis on a semiconductor device under inspection, comprising preparing of a sample of the semiconductor device under inspection using an encapsulation material containing a dye, the prepared device sample possibly including at least one failure area containing wicked in encapsulation material containing the dye (see fig 1 – the semiconductor device, 120, is soaked in dye, 150, and dried in a vacuum, fig 2 – 210, the areas with bumps or defects are shown in fig 3 – 320 indicated as D showing that the dye had flowed it's way into the crack defect), but does not disclose sectioning the prepared device.

However, the background section of DePetrillo shows it is a conventional inspection technique to involve cross-sectioning an assembled circuit board (see col. 1 lines 40 – 41). Since the cross sectioning in the claimed invention is to detect defects (eg. cracks) on semiconductor device and not solder bumps, it is

advantageous for the claim invention to use cross sectioning to locate cracks on semiconductor device. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include cross sectioning on semiconductor face during inspection because it allows the operator to find area of defects within the semiconductor to find cracks within the semiconductor to take early actions to remedy the crack from within before it opens our on the surface of the said semiconductor device.

DePetrillo discloses dye be photographed with white light (see col. 3 lines 14 – 16), wherein responsive to at least one failure area containing wicked in encapsulation material with dye occurring on the cross section face of the device under inspection (see fig 3 – 320 – shows a cross section of the semiconductor device with dye wicked into the defect areas), the failure area can be readily identified as well as a contrast and perspective of remaining portions of the cross section face being maintained (see col. 3 lines 14 – 16 – uses white light to locate the defects), but does not use dark field illumination to analyze the dye wicked into the failure area.

Nishimura discloses dark field illumination to detect defects in semiconductor device (see col. 8 lines 32 – 36 – the dark portions shown in fig 3 are areas under dark illumination and the bright part are the circuit area, the defect area shows up within the brighter areas). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include dark field illumination to locate the dye within the defects / cracks because the dye will

show up white and bright to the observer or camera (see Nishimura fig 1 – 10), so the operator may be able to gather a solution to remedy the crack.

With regards to claim 2, DePetrillo discloses a method of claim 1, wherein the semiconductor device includes a wafer level chip scale packaged semiconductor device (see fig 1).

With regards to claim 4, DePetrillo discloses a method of claim 1, wherein the dye includes a dye pigment that is added to an uncured epoxy encapsulation material (see fig 1 – 110).

With regards to claim 5, DePetrillo discloses a method of claim 4, wherein preparing the device sample further includes placing the sample into a container along with the uncured epoxy containing the dye pigment, placing the same in a vacuum chamber, and maintaining the same under vacuum within the vacuum chamber for a duration of time sufficient for allowing the uncured epoxy encapsulation material containing dye to wick into a failure area of delaminating extending from an exterior to an interior of the device sample (see fig 1 – 140 is the container where the semiconductor device is being placed within dye, 14 and then being put in a vacuum, fig 2 – 210, fig 3 shows the dye had flowed into the defect area).

With regards to claim 6, DePetrillo discloses a method of claim 5, further including configuring the conditions within the vacuum chamber to promote wicking of the encapsulation material containing dye into the failure area (see fig 2 – 210).

With regards to claim 7, DePetrillo discloses a method of claim 5, wherein preparing the device sample further includes employing a vacuum purge cycle subsequent to placing the device sample under vacuum within the vacuum chamber for the duration of wicking, allowing the dye and encapsulation material to return to standard ambient conditions, and then curing the encapsulation material containing the dye (see fig 3 – shows the dye being dried, fig 2 – 240, and shows the location of defects and see fig 2 – 210 for areas being under vacuum).

With regards to claim 8, DePetrillo discloses a method of claim 4, further wherein the encapsulation material includes a two component encapsulant comprised of a resin (see fig 1 – 110) and a hardener (see col. 3 lines 25 – 30 – when the dye dries will harden).

With regards to claim 10, DePetrillo and Nishimura disclose a method of claim 1, wherein performing the dark field analysis includes capturing an image of the cross section of the prepared device sample under dark field illumination (see the rationale for claim 1).

With regards to claim 11, DePetrillo and Nishimura disclose a method of claim 1, further wherein performing the dark field analysis includes using a compound microscope configured for dark field illumination and inspection and wherein the compound microscope includes an image capture system coupled to the compound microscope for capturing an image of the cross section face of the device under inspection (see the rationale for claim 1 and see col. 3 lines 14 – 15 and 46).

With regards to claim 12, DePetrillo discloses all of the claim elements / features as discussed above in rejection for claim 11 and incorporated herein by reference, but fails to disclose captured image include a digital image. Nishimura discloses a method of claim 11, wherein the captured image includes a digital image (see fig 1 – 10). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include captured image is a digital image because to allow faster computing, which analyzes pixels data locating the defect areas within the imaged semiconductor ship saving processing time.

With regards to claim 13, DePetrillo discloses a method of claim 1, wherein the dark field illumination includes use of a full complement of light for illuminating the cross section face of the device under inspection (see col. 3 line 15).

With regards to claim 16, see the rationale and rejection for claim 1.

With regards to claim 17, see the rationale and rejection for claim 2.

With regards to claim 19, see the rationale and rejection for claim 4.

With regards to claim 20, see the rationale and rejection for claim 5.

With regards to claim 21, see the rationale and rejection for claim 11.

With regards to claim 24, see the rationale and rejection for claim 1. In addition, DePetrillo claimed invention is related to a method for testing the integrity of soldered joints in semiconductor package assemblies, implying that it will not package the semiconductor device if it contains defects, therefore further examination of the semiconductor is necessary.

With regards to claim 25, DePetrillo discloses a method of claim 24, wherein the device includes at least one selected from the group consisting of a semiconductor device and a printed circuit board (see fig 3).

With regards to claim 26, see the rationale and rejection 3.

With regards to claim 27, DePetrillo discloses a method of claim 24, wherein the process component includes at a solder mask (see fig 7).

With regards to claim 28, see the rationale for claim 1 and 24. In addition, DePetrillo shows in fig 3 the residue are left in the defective solder and semiconductors are in size angstroms when viewing each individual solder holes.

With regards to claims 29 and 30, see the rationale and rejection for claim 24.

3. Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over DePetrillo (US pat no 6,342,400) in view of Nishimura (US pat no 5,761,337) as applied to claim 1 further in view of Forest (US pat no 2,806,959).

With regards to claim 3, DePetrillo discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose 3. The method of claim 1, wherein the dye includes at least one fluorescent dye selected from the group consisting of a Xanthane, Naphthalimide, Perylene, Courmarin, and Fluorescein based family. Forest discloses the dye includes at least one fluorescent dye selected from the group consisting Perylene (see col. 4 lines 57 – 62). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include Perylene fluorescent based dye because Perylene has low viscosity which,

allows the dye to easily penetrate into the crack defect area, so the operator can see where the location of the failure.

With regards to claim 18, see the rationale and rejection for claim 3.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over DePetrillo ('400) in view of Nishimura ('337) as applied to claim 1 further in view of Rubin (US pat no 6,781,232) and Forest ('959).

With regards with claim 9, DePetrillo discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose grinding and polishing. Forest suggests clearing the dye using water shown in fig 3. One would clear the dye layer because find the exact location of the crack as shown in fig 6 of Forest, where the crack is clearly shown after the clearing the dye with water. But Forest does not use grinding and polishing to clear upper layer of dye. Rubin discloses grinding and polishing on a target area on a semiconductor device (see col. 2 lines 50 – 52). One would use grinding and polishing on a selected area of a semiconductor device because to remove a very precise amount of material in a minimal amount of time benefiting the operator when examining a multitude of semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex Liew whose telephone number is (571)272-8623. The examiner can normally be reached on 9:30AM - 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on (571)272-7695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alex Liew
AU2624
10-17-06

JOSEPH MANCUSO
SUPERVISORY PATENT EXAMINER